Remarks

The amendment set forth above is being filed with a Request for Continued Examination (RCE) in the subject case pursuant to 37 CFR 1.114. This amendment and request are provided in response to an Office Action dated 12/31/2002 that was made FINAL ("Final Rejection") in which Claims 1-20 were rejected. In the amendment, Claim 1 is amended, Claims 6-7 remain as previously presented, Claims 8-20 are canceled, and Claims 21-46 are newly presented. In view of the Amendments to the Claims and the comments set forth below, it is respectfully submitted that the Claims as currently presented are allowable over the references cited in the Final Rejection, and an early Notice of Allowance is respectfully requested.

1. In the Final Rejection, Claims 1 was rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 5,325,495 to McLellan ("McLellan").

Before addressing the language of amended Claim 1, the McLellan system is summarized for discussion purposes. McLellan discloses a pipeline having first pipeline stages 1-3, an intermediate Q stage, and a pipeline stage 4. Instructions are passed between the third and fourth stages via the Q stage. When a stall occurs in the fourth or subsequent stage of the pipeline, the Q stage is inserted into the pipeline to store an instruction received from stage 3. Thereafter, the Q stage is included as an additional stage within the pipeline as follows:

> "According to the invention, in the control stages, a queue stage 16 is added before the stage #4, receiving the output 17 from the stage #3 under certain conditions." (McLellan column 5 lines 26-29.)

This additional stage remains included within the pipeline until a "bubble" is created within one of the first pipeline stages, resulting in removal of the Q stage from the pipeline as follows:

> "When a bubble enters the queue stage 16 (or the queue stage is empty), the multiplexer 18 switches back to accepting output from stage #3, thus allowing the pipeline to go back to being a four stage pipeline instead of a five stage pipeline by omitting the queue stage." (McLellan column 5 lines 59-64.)

As can be appreciated from the foregoing discussion, McLellan inserts a Q stage between the third and fourth stages of a pipeline when a stall occurs in one of the latter pipeline stages. This Q stage does not perform any useful processing task, but rather just stores an instruction. This stage therefore inserts a delay that causes any given instruction that enters the pipeline to be executed more slowly.

Next, the McLellan pipeline is compared to Applicants' pipeline circuit of amended Claim 1. In the Final Rejection, the Examiner correlates the first stages of the McLellan pipeline to Applicants' fetch stages, and the fourth and subsequent stages of the McLellan pipeline to Applicants' execution stages. The Examiner further states that the first stages of the McLellan pipeline are coupled directly to the last McLellan stages via the Q stage. These analogies will be accepted for discussion purposes only in reference to Applicants' Claim 1.

Amended Claim 1 includes a pipeline execution circuit to process a first predetermined number of instructions simultaneously, each being in a respectively different stage of execution within the pipeline execution circuit. Claim 1 further includes a pipeline fetch circuit coupled to provide *each of these first predetermined number of instructions directly* to said pipeline execution circuit. An instruction is capable of advancing to a next stage of execution within the pipeline fetch circuit at a time determined by the system clock signal and independently of the times at which instructions advance to a next stage of execution within the pipeline execution circuit.

According to the foregoing, Applicants' Claim 1 includes a pipeline fetch circuit that *directly* provides *each of the instructions* that is executed by the execution circuit. This is in contrast to the McLellan system, wherein the early

pipeline stages must, at times, provide instructions to the later stages indirectly through the Q stage. This introduces a delay of at least one additional clock cycle into the pipeline that is not introduced by Applicants' pipeline circuit. For at least this reason, amended Claim 1 is not taught or suggested by McLellan.

2. In the Final Rejection, Claims 2-6 were rejected under 35 USC § 103(a) as being unpatentable over McLellan in view of U.S. Patent No. 5,778,423 to Sites et al. ("Sites").

Claims 2-6 depend from Claim 1. Sites adds nothing to McLellan that would teach or suggest the limitations of Applicants' Claim 1. Therefore, Claims 2-6 are allowable over this rejection for at least the reasons discussed above in reference to Claim 1. These Claims further include additional scopes and aspects not taught or suggested by the cited combination of references. For these reasons, Claims 2-6 are allowable over the cited references as currently presented. Applicants maintain that the various features described in these Claims are not inherent to all pipeline designs, as is argued by the Examiner in pages 22-25 of the Final Rejection.

3. In the Final Rejection, Claim 7 was rejected under 35 USC § 103(a) as being unpatentable over McLellan in view of U.S. Patent No. 5,577,259 to Alferness et al. ("Alferness"). Alferness does not add anything to McLellan to teach or suggest the limitations of Applicants' Claim 1. For at least this reason, Claim 7 is allowable over the cited references.

4. Claims 8-20 have been canceled in the foregoing Amendment.

5. Claims 21-46 are newly presented in the Amendment. These Claims include aspects similar to those discussed above in reference to Applicants' Claim 1. For example, Claim 21 includes an execution circuit to provide a first predetermined number of execution stages, each being capable of performing a

respective processing operation on a respective instruction. Claim 21 further includes a fetch circuit coupled to the execution circuit to provide a second predetermined number of fetch stages. The fetch circuit transfers *each* instruction processed by the fetch stages *directly from one of the fetch stages to one of the execution stages*. Ones of the instructions processed within the fetch stages are capable of advancing to different available fetch stages independently of whether instructions are advancing within the execution stages.

Applicants' Claim 21, like Claim 1, describes a fetch circuit that transfers each instruction processed by the fetch circuit directly from a fetch stage to an execution stage without inserting an unnecessary intermediate stage, as is taught by McLellan. For at least this reason, Claim 21 is not taught or suggested by McLellan.

Dependent Claims 22-26 depend from Claim 21, and describe additional aspects of Applicants' invention not taught or suggested by McLellan, or any of the other cited references, alone or in combination. Applicants' maintain that these additional aspects are not necessarily inherent to pipeline designs generally, as stated by the Examiner in pages 22-25 of the Final Rejection.

Claims 27-46 include scopes and aspects similar to those discussed above in reference to Claims 1-7 and 21-26. These Claims are likewise allowable over the cited references.

Conclusion

The amendment set forth above is being filed with a Request for Continued Examination (RCE) in the subject case pursuant to 37 CFR 1.114. This amendment and request are provided in response to an Office Action dated 12/31/2002 that was made FINAL in which Claims 1-20 were rejected. In view of the newly presented Claims, and the comments set forth above, it is respectfully submitted that the Claims, as currently presented, are allowable over the references cited in the Final Rejection, and an early Notice of Allowance is respectfully requested. If the Examiner has any questions or concerns regarding this submission, a call to the undersigned is welcomed and encouraged.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.10: The undersigned hereby certifies that this transmittal letter and the paper of papers, as described hereinabove, are being deposited in the United States Postal Service, "Express Mail Post Office to Addressee" having an Express Mail mailing label number of EU039120477US, in an envelope addressed to: COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231 on this 30th day of April 2003.

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